Multi-Mission MicroSDR, Phase I

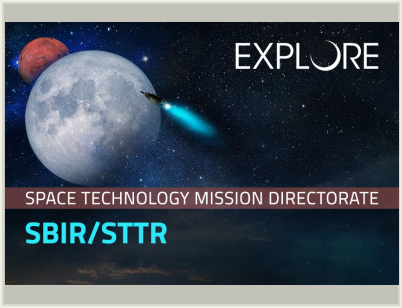
Completed Technology Project (2007 - 2007)

Project Introduction

Toyon proposes to develop a low-power and compact reconfigurable radio specifically targeted to NASA mission needs. We envision the radio to be well matched to small satellites, terrestrial ground links, and autonomous vehicles. The design is based on the latest in field programmable gate array (FPGA) and general purpose processors (GPP). Typical software defined radios (SDRs) rely heavily on digital signal processors (DSPs) due to their ease of software development and ability to multitask well. Our emphasis will be on performing all baseband processing inside the FPGA due to its ability to offer over an order of magnitude increase in computational efficiency. While this approach does significantly decrease power consumption and associated platform size, it requires special considerations, particularly in terms of software development. As such, we will leverage Toyon's ongoing experience in computationally efficient waveform and associated software development using the latest in FPGA behavioral design tools. In addition, the architecture will stress logic component reuse between multiple waveforms to support rapid reconfiguration as well as reduce development time. Our RF front-end design will be a direct-conversion architecture to reduce size and provide frequency agility. The use of open-standards interfaces will provide for rapid systems integration.

Anticipated Benefits

With a desire to reconfigure and reuse wireless equipment, there is tremendous interest in SDR for the military, emergency response, and consumer applications. At the same time, numerous factors have limited its penetration into these markets. With the military's ability to combine a large number of radios into a single package, JTRS does have potential; this is particularly true for its use in larger platforms that are not constrained in size and power. However, integrating SDR technology into smaller equipment, that is cost and power constrained, will require the use of more computationally efficient processing and considerations on overall architecture. The proposed concept is specifically targeted to these requirements by leveraging FPGA processing and direct-conversion RF translation. At the same time, our goal will be to exploit logic and processing reuse in order to allow rapid reconfiguration for the support of multiple waveforms.



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Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Center / Facility:

Glenn Research Center (GRC)

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

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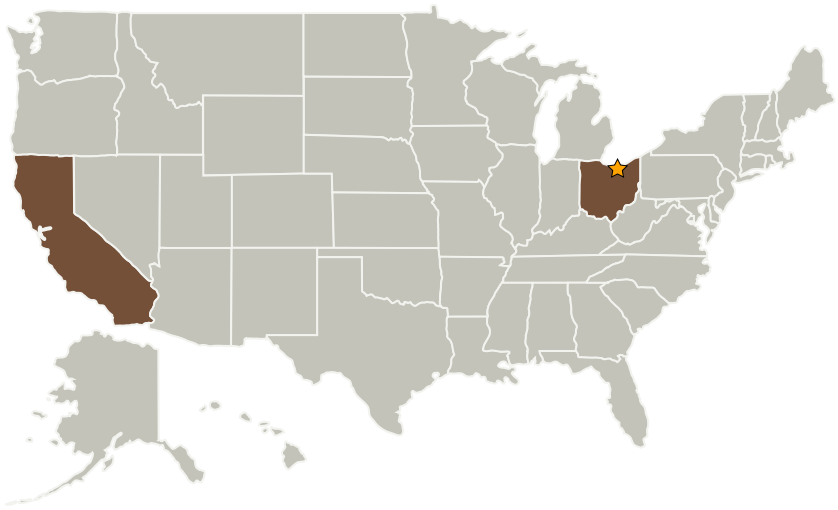
Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
★Glenn Research Center(GRC)	Lead Organization	NASA Center	Cleveland, Ohio
Toyon Research Corporation	Supporting Organization	Industry	Goleta, California

Primary U.S. Work Locations	
California	Ohio

Project Management

Program Director:
Jason L Kessler

Program Manager:
Carlos Torrez

Project Manager:
Monty Andro

Principal Investigator:
Richard Cagley

Technology Areas

Primary:

- TX02 Flight Computing and Avionics
  - TX02.1 Avionics Component Technologies
    - TX02.1.5 High Performance Field Programmable Gate Arrays